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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,913	03/30/2004	Paul Hanrieder	57983.000165	3176

21967 7590 12/27/2006

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EXAMINER	
BAE, JI H	
ART UNIT	**PAPER NUMBER**
2115	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/27/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/811,913	HANRIEDER ET AL.	
	Examiner	Art Unit	
	Ji H. Bae	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed on 16 October 2006 have been fully considered but they are not persuasive.

Regarding the obviousness rejection of claims 1-20, the applicant's attorney has argued that the examiner has failed to establish a prima facie case of obviousness. In particular, applicant's attorney has alleged that the examiner has failed to demonstrate how the combination of Strasser and Taylor teaches all the claimed limitations. In the original office action, the examiner cited Strasser as teaching the claimed memory configuration, as well as a controller that controls the transferring of data from a volatile memory to a non-volatile memory when voltage is above a minimum [non-final office action, pp. 3-4, mailing date 7/14/2006]. Strasser teaches these limitations in col. 7, lines 26-41 and in Fig. 4. Taylor was cited as teaching the missing limitation of monitoring data storage changes, for example in col. 8, lines 16-18 and col. 8, line 59 to col. 9, line 16. On page 12 of applicant's remarks, applicant's attorney has argued that Taylor does not teach the monitoring of data storage changes made within the volatile memory, and that in fact, Taylor teaches away from the claimed limitation by "eliminating the claimed feature of transferring data stored in the volatile memory to the non-volatile memory based on monitored data storage changes."

In response, the examiner points out that both Strasser and Taylor are directed towards solving similar problems using a similar configuration. Specifically, both Strasser and Taylor teach a memory configuration composed of a volatile memory and a non-volatile memory, wherein the contents of the volatile memory are to correspond to what is stored in the non-volatile memory and vice versa. The applicant's argument that Taylor does not teach the transferring step is irrelevant since Taylor is not relied upon to reject that feature. Strasser is

cited as teaching the limitation of transferring data from volatile to non-volatile memory. Moreover, because Strasser teaches that the transferring step is repeated periodically [col. 7, lines 29-31], it is clear that Strasser does not teach that transferring is done in response to monitoring data storage changes, but rather that the transferring is carried out automatically on a periodic basis.

Taylor is cited as teaching a write through caching mechanism wherein, upon a cache hit, the contents of the non-volatile memory are updated to reflect what is written to the volatile memory. In particular, the examiner points out that in a write through caching scheme, writes to the volatile memory are reflected to the non-volatile memory only on a cache hit – in other words, the non-volatile memory is updated only when the volatile memory is written to, not on a repeated, periodic basis as is taught by Strasser.

Thus, the examiner asserts that, in view of the disclosures of both Taylor and Strasser, it would have been obvious to one of ordinary skill in the art to modify Strasser to implement a monitoring scheme similar to the write though caching policy of Taylor, in order to carry out the transferring step previously taught by Strasser, in response to a write to the volatile memory as taught by Taylor. The teachings of Taylor would improve Strasser by obviating the need for a repeated, periodic update. Instead the non-volatile memory would only be written to when the volatile memory is written.

Strasser teaches that the non-volatile memory may constitute flash memory [col. 4, line 15]. It is generally known in the art that flash memories have a limited number of erase and write cycles before the part becomes unreliable [Pfeiffer and Ayre, "Using Flash Memory in Embedded Applications"]. Therefore, one of ordinary skill in the art would have been motivated to limit the number of write cycles to the non-volatile memory of Strasser. As such, the teachings of Taylor regarding the update of the non-volatile memory only when the volatile

memory is written to represents an improvement over Strasser by reducing the number of writes to the non-volatile memory, thus prolonging its useful lifetime.

The examiner further points out that this motivation cannot be construed as hindsight reasoning, since applicant's specification nowhere discusses the desire to prolong the useful lifetime of flash memories.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Strasser, U.S. Patent No. 6,990,603, in view of Taylor et al., U.S. Patent No. 6,263,398 B1.

Regarding claim 1, Strasser teaches:

a high speed volatile memory [Fig. 1, volatile memory 220];

a non-volatile memory coupled to the high speed volatile memory [non-volatile memory 230];

a controller coupled to the high speed volatile memory and the non-volatile memory that controls transfer of data from the high speed volatile memory to the non-volatile memory when power is above a particular minimum operating voltage level [control unit 210, also Fig. 4, col. 7, lines 26-37]; and

a power level detector that detects when power is above the minimum operating voltage level [col. 7, lines 39-41].

Strasser does not teach that the controller monitors data storage changes made in the high speed volatile memory.

Taylor teaches a memory system employing a non-volatile memory coupled to a cache [Fig. 1], employing a "write-through" caching technique. The system monitors writes to the cache and reflects the changes made to the cached data in the non-volatile memory [col. 8, lines 16-18, 59 to col. 9, line 16].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Strasser and Taylor by modifying the controller of Strasser to monitor for data changes in the volatile memory, as taught by Taylor. Both Strasser and Taylor teach memory systems comprised of a volatile memory and a slower, non-volatile memory that holds a copy of the data in the volatile memory. Strasser teaches that the backing up of the volatile memory occurs periodically while the minimum power is maintained, but does not how often. The teachings of Taylor would improve the system of Strasser by triggering writes to the non-volatile memory upon detecting changes to the volatile memory (e.g. write through), thus ensuring that the non-volatile memory accurately reflects the latest changes made to the volatile memory.

Regarding claim 2, Strasser teaches a power storage element that stores transient power for use by at least one of the high speed volatile memory, the non-volatile memory, and the controller when power is below the particular minimum operating voltage level [uninterruptible power supply 240, Fig. 2].

Regarding claim 3, Strasser teaches that the power from the power storage element is used to transfer the stored data in the volatile memory to the non-volatile memory when power is below the particular minimum operating level [col. 5, lines 48-50].

Regarding claim 4, it would have been obvious to use a capacitor with capacitance in the hundred of microfarads as a matter of design choice.

Regarding claim 5, it would have been obvious to use a dynamic RAM for the high speed volatile memory. DRAM is a well-known and commonly used volatile memory.

Regarding claim 8, Taylor teaches that the non-volatile memory is a low speed non-volatile memory relative to the high speed volatile memory [col. 2, lines 30-33].

Regarding claim 9, Strasser teaches that the non-volatile memory is a non-volatile flash memory [claim 19].

Regarding claim 10, Strasser teaches that the controller is one of a microprocessor, a microcontroller, a programmable processing device, and a fixed function processing device [claim 17].

Regarding claim 11, Strasser teaches that the controller prevents the transfer of stored data from the high speed volatile memory to the non-volatile memory, and vice versa, when power is below the particular minimum operating voltage level [UPS shut down, col. 8, lines 1-5].

Regarding claim 12, Strasser teaches that the controller controls the transfer of stored data from the non-volatile memory to the high-speed volatile memory immediately following a restoration of power to above the particular minimum operating voltage level [col. 9, lines 10-23].

Regarding claim 13, Strasser teaches that the power level detector provides an indication to the controller that power is above the particular minimum operating voltage level.

Regarding claim 14, Strasser/Taylor teaches a method comprising:

monitoring data storage changes made within a high speed volatile memory [col. 8, lines 16-18, 59 to col. 9, line 16];

permitting stored data to be transferred from the high speed volatile memory to a non-volatile memory, and vice versa, based upon the monitored data storage changes when power is above a particular minimum operating voltage level [col. 7, lines 26-37]; and

preventing stored data to be transferred from the high speed volatile memory to the non-volatile memory, and vice versa, when power is below the particular minimum operating voltage level [UPS shut down, col. 8, lines 1-5].

Regarding claim 15, Strasser teaches detecting when power is above the particular minimum operating voltage level.

Regarding claim 16, Strasser teaches providing an indication that power is above the particular minimum operating voltage level.

Regarding claim 17, Strasser teaches detecting when power is below the particular minimum operating voltage level.

Regarding claim 18, Strasser teaches providing an indication that power is below the particular minimum operating voltage level.

Regarding claim 19, Strasser teaches providing a transient power when power is below the particular minimum operating voltage level [uninterruptible power supply 240, Fig. 2]; and

permitting stored data to be transferred from the high speed volatile memory to a non-volatile memory based upon the monitored data storage changes for a limited period of time using the transient power when power is below the particular minimum operating voltage level [col. 5, lines 48-50].

Regarding claim 20, Strasser teaches controlling the transfer of stored data from the non-volatile memory to the high speed volatile memory immediately following a restoration of power to above the particular minimum operating voltage level [col. 9, lines 10-23].

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ji H. Bae whose telephone number is 571-272-7181. The examiner can normally be reached on Monday-Friday, 10 am to 6:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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